Datasheet

G32M3101x8

Arm® Cortex® -M0+ core-based 32-bit SoC

Version: V1.3

1 Product Characteristics

Core

- 32-bit Arm® Cortex®-M0+ core
- Up to 64MHz working frequency

Memory and interface

- Flash: Up to 64KB
- SRAM: 8KB

Clock

- HSICLK: Built-in 64MHz high-frequency RC oscillator
- LSICLK: Built-in 32.768KHz low-frequency RC oscillator

Power and power management

- V_{BB} range: 5~36V
- V_{DD5} range: 5V
- Support power-on/power-off (POR/PDR）
- Support programmable voltage detector (PVD)

Low power mode

- Support sleep and stop modes

DMA

- 1 DMA with 3 channels

Debugging interface

- SWD

I/O

- Up to 24 I/O
- All I/Os can be mapped to external interrupt vectors
- Up to 24 I/O tolerating 5V inputs

Communication peripherals

- 2 UART, support LIN function
- 1 SPI

Analog peripherals

- 1 12-bit ADC, support up to 8+2 external channels and 6 internal channels, with conversion range from 0V~5V. Maximum sampling rate 2 MSPS
- 2 programmable analog comparators (COMP)
- 2 rail-to-rail operational amplifiers (OPAMP)

Timer

- 1 16-bit advanced timer that can provide 8-channel PWM output, support for deadband generation and brake inputs
- 1 32-bit general-purpose timer with 4 independent channels for input capture, output comparison, PWM and pulse counting
- 1 16-bit basic timer
- 1 16-bit low-power timer
- 2 watchdog timers: an independent watchdog IWDT and a window watchdog WWDT
- 1 24-bit self-reducing SysTick Timer

Algorithm unit

- CRC
- DIV

Built-in 3P+3N gate driver

- HO/LO, rising edge/falling edge, and four output slopes can be independently selected
- Output current of HO

  +320mA/-70mA@Vsup=24V
- LO Output current

  +60mA/-210mA@Vsup=24V
- Built-in 5V/60mA LDO
- Built-in deadband time of 240ns
- Built-in under-voltage protection/anti-direct current function

96-bit unique device ID

Chip package

- LQFP32
- QFN32
- SSOP28
- SSOP24

Contents

2 Product Information

See the following table for G32M3101 product functions and peripheral configuration.

Table 1 Functions and Peripherals

Product		**G32M3101**			
Model		K8Ux	K8Tx	G8Sx	E8Sx
Package		QFN32	LQFP32	SSOP28	SSOP24
Core and maximum working frequency		Arm® 32-bit Cortex®-M0+@64MHz			
Working voltage (Built-in drive voltage)		5~36V			
SoC Working voltage		2.7~5.5V			
Flash (KB)		64			
SRAM (KB)		8			
DMA		1			
GPIOs		24	23	19	15
Algorithm units	CRC	1			
	DIV	1			
Timers	16-bit advanced (ATMR)	1			
	32-bit general (GTMR)	1			
	16-bit basic (BTMR)	1			
	24-bit SysTick (SYSTICK)	1			
	Watchdog	2（IWDT+WWDT）			
	LPTMR	1			
Communication interfaces	UART	2			
	SPI	1			
12-bit ADC	Unit	1			
	External channel	8+2	8+2	4+2	3+2
	Internal channel	6			
Comparator		2	2	1	1
Operational amplifier (OPAMP)		2			
Temperature sensor		1			
Gate driver		3P+3N			
Withstand voltage of the drive power supply		40V			
Built-in LDO		5V			
Operating temperature		Ambient temperature: -40℃ to 85℃/-40℃ to 105℃			

Product	G32M3101
	Junction temperature: -40℃ to 105℃/-40℃ to 125℃

Notes：

（1） When x is 6, the ambient temperature is -40℃ to 85℃, and the junction temperature is -40℃ to 105℃.

When x is 7, the ambient temperature is -40℃ to 105℃, and the junction temperature is -40℃ to 125℃.

3 Pin Information

3.1 Pin distribution

Figure 1 LQFP32 Pin Distribution Diagram

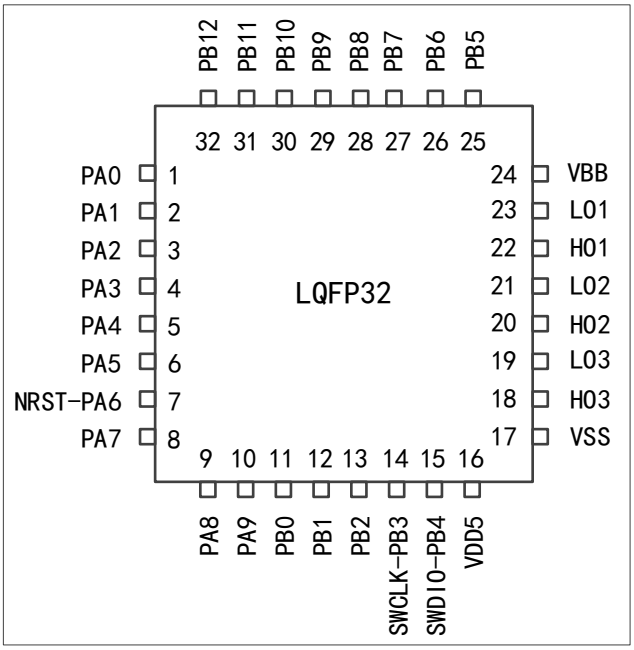


Figure 2 QFN32 Pin Distribution Diagram

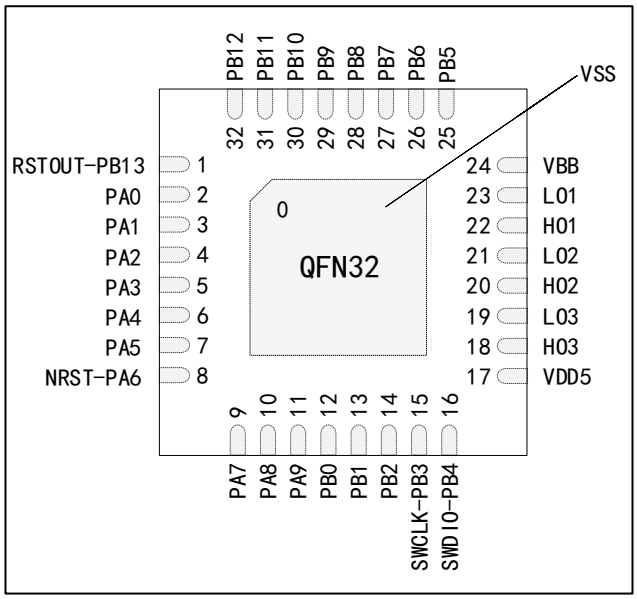


Figure 3 SSOP28 Pin Distribution Diagram

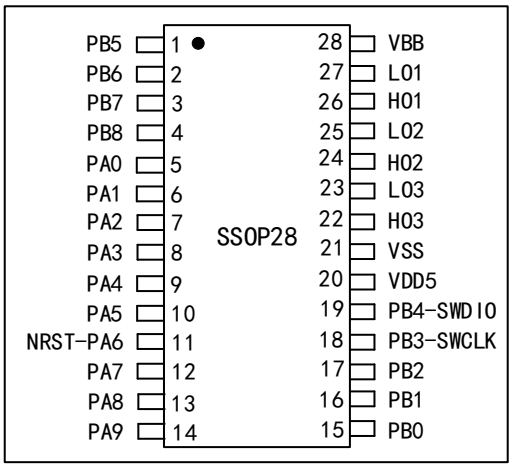
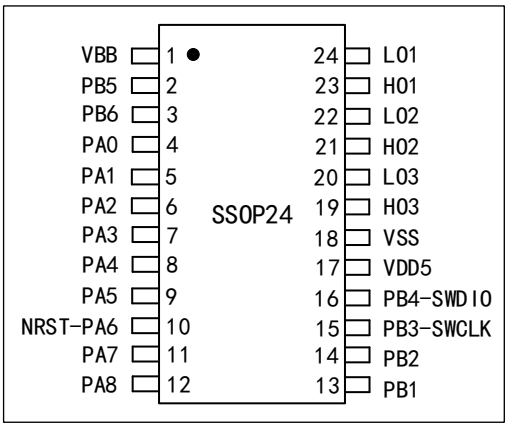


Figure 4 SSOP24 Pin Distribution Diagram



3.2 Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power pin
	I	Only input pin
	O	Only output pin
	I/O	I/O pin
I/O structure	5T	5V tolerant FT I/O
	STDA	3.3V standard I/O, directly connected to ADC
	STD	3.3V standard I/O
	B	Dedicated Boot0 pin

Name		Abbreviation	Definition
		RST	One-way reset pin with built-in pull-up resistor
Notes		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Select this function through AFIO remapping registers	
	Additional function	Select this function directly through peripheral registers	

Table 3 Descriptions by Pin Number

LQFP32	QFN32	SSOP28	SSOP24	Pin Name (After reset)	Digital Multiplexing Function	Analog Multiplexing Function	Type
1	2	5	4	PA0	-	OPAMP0_OUT COMP1_INP ADC_IN12	I/O
2	3	6	5	PA1	-	OPAMP0_INN COMP1_INN0	I/O
3	4	7	6	PA2	-	OPAMP0_INP COMP1_INN1	I/O
4	5	8	7	PA3	-	OPAMP1_INP	I/O
5	6	9	8	PA4	-	OPAMP1_INN	I/O
6	7	10	9	PA5	-	OPAMP1_OUT COMP0_INP COMP1_INN2 ADC_IN13	I/O
7	8	11	10	NRST (PA6)	NRST	-	I/O
8	9	12	11	PA7	UART0_TX, ATMR_BKIN, GTMR_CH0_ETR, CLKOUT	ADC_IN0 COMP0_INP	I/O
9	10	13	12	PA8	UART0_RX, ATMR_ETR, GTMR_CH1	ADC_IN1 COMP0_INN0	I/O
10	11	14	-	PA9	UART1_TX, SPI_CS, ATMR_CH3, GTMR_CH2, COMP0_OUT	COMP0_INN1	I/O
11	12	15	-	PB0	UART1_RX, SPI_SCK, ATMR_CH4, GTMR_CH3, BTMR_CH0	COMP0_INN2	I/O

LQFP32	QFN32	SSOP28	SSOP24	Pin Name (After reset)	Digital Multiplexing Function	Analog Multiplexing Function	Type
12	13	16	13	PB1	UART0_TX, SPI_MOSI, ATMR_BKIN, GTMR_CHO_ETR, COMP1_OUT	ADC_IN4 COMP0_INN3 VREF+	I/O
13	14	17	14	PB2	UART0_RX, SPI_MISO, ATMR_ETR, GTMR_CH1	ADC_IN5 COMP0_INN4	I/O
14	15	18	15	SWCLK (PB3)	SWCLK, UART0_TX, ATMR_CH3, GTMR_CH2, BTMR_CH1	ADC_IN6 COMP1_INP	I/O
15	16	19	16	SWDIO (PB4)	SWDIO, UART0_RX, ATMR_CH4, GTMR_CH3, BTMR_CH2	ADC_IN7 COMP1_INN0	I/O
16	17	20	17	VDD5	LDO 5V output, connect 4.7uF and 100nF capacitors to ground	-	P
17	-	21	18	VSS	Chip ground	-	P
18	18	22	19	HO3	-	-	O
19	19	23	20	LO3	-	-	O
20	20	24	21	HO2	-	-	O
21	21	25	22	LO2	-	-	O
22	22	26	23	HO1	-	-	O
23	23	27	24	LO1	-	-	O
24	24	28	1	VBB	Power supply voltage input	-	P
25	25	1	2	PB5	UART1_TX, SPI_CS, GTMR_CH2, BTMR_CH0, COMP0_OUT	ADC_IN2, COMP1_INN1	I/O
26	26	2	3	PB6	UART1_RX, SPI_SCK, GTMR_CH3, BTMR_CH1,	ADC_IN3, COMP1_INN2	I/O

LQFP32	QFN32	SSOP28	SSOP24	Pin Name (After reset)	Digital Multiplexing Function	Analog Multiplexing Function	Type
					COMP0_OUT		
27	27	3	-	PB7	UART1_TX, SPI_MISO, BTMR_CH2, COMP1_OUT	COMP0_INP	I/O
28	28	4	-	PB8	UART1_RX, SPI_MOSI, COMP1_OUT	COMP1_INP	I/O
29	29	-	-	PB9	UART0_TX, SPI_CS, ATMR_BKIN, GTMR_CH0_ETR, BTMR_CH0	-	I/O
30	30	-	-	PB10	UART0_RX, SPI_SCK, ATMR_ETR, GTMR_CH1, BTMR_CH1, COMP0_OUT	-	I/O
31	31	-	-	PB11	SPI_MISO, ATMR_CH3, GTMR_CH2, BTMR_CH2, COMP1_OUT	-	I/O
32	32	-	-	PB12	SPI_MOSI, ATMR_CH4, GTMR_CH3	-	I/O
-	1	-	-	RSTOUT (PB13)	RSTOUT	-	I/O

3.3 GPIO multiplexing configuration

Table 4 Multiplexing configuration for port A

	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Analog
PA0	-	-	-	-	-	-	-	-	OPAMP0_OUT COMP1_INP ADC_IN12
PA1	-	-	-	-	-	-	-	-	OPAMP0_INN COMP1_INN0
PA2	-	-	-	-	-	-	-	-	OPAMP0_INP COMP1_INN1
PA3	-	-	-	-	-	-	-	-	OPAMP1_INP

	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Analog
PA4	-	-	-	-	-	-	-	-	OPAMP1_INN
PA5	-	-	-	-	-	-	-	-	OPAMP1_OUT COMP0_INP COMP1_INN2 ADC_IN13
PA6	-	-	-	-	-	-	-	NRST(default)	-
PA7	UART0_TX	-	-	ATMR_BKIN	GTMR_CH0_ETR	-	-	CLKOUT	ADC_IN0 COMP0_INP
PA8	UART0_RX	-	-	ATMR_ETR	GTMR_CH1	-	-	-	ADC_IN1 COMP0_INN0
PA9	UART1_TX	SPI_CS	-	ATMR_CH3	GTMR_CH2	-	-	COMP0_OUT	COMP0_INN1

Table 5 Multiplexing configuration for port B

	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Analog
PB0	UART1_RX	SPI_SCK	-	ATMR_CH4	GTMR_CH3	BTMR_CH0	-	-	COMP0_INN2
PB1	UART0_TX	SPI_MOSI	-	ATMR_BKIN	GTMR_CH0_ETR	-	-	COMP1_OUT	ADC_IN4 COMP0_INN3 VREF+
PB2	UART0_RX	SPI_MISO	-	ATMR_ETR	GTMR_CH1	-	-	-	ADC_IN5 COMP0_INN4
PB3	SWCLK	UART0_TX	-	ATMR_CH3	GTMR_CH2	BTMR_CH1	-	-	ADC_IN6 COMP1_INP
PB4	SWDIO	UART0_RX	-	ATMR_CH4	GTMR_CH3	BTMR_CH2	-	-	ADC_IN7 COMP1_INN0
PB5	UART1_TX	SPI_CS	-	-	GTMR_CH2	BTMR_CH0	-	COMP0_OUT	ADC_IN2 COMP1_INN1
PB6	UART1_RX	SPI_SCK	-	-	GTMR_CH3	BTMR_CH1	-	COMP0_OUT	ADC_IN3 COMP1_INN2
PB7	UART1_TX	SPI_MISO	-	-	-	BTMR_CH2	-	COMP1_OUT	COMP0_INP
PB8	UART1_RX	SPI_MOSI	-	-	-	-	-	COMP1_OUT	COMP1_INP
PB9	UART0_TX	SPI_CS	-	ATMR_BKIN	GTMR_CH0_ETR	BTMR_CH0	-	-	-
PB10	UART0_RX	SPI_SCK	-	ATMR_ETR	GTMR_CH1	BTMR_CH1	-	COMP0_OUT	-
PB11	-	SPI_MISO	-	ATMR_CH3	GTMR_CH2	BTMR_CH2	-	COMP1_OUT	-
PB12	-	SPI_MOSI	-	ATMR_CH4	GTMR_CH3	-	-	-	-
PB13	-	-	-	-	-	-	-	RSTOUT (default)	-

Table 6 Gate Driver Internal Wiring Mapping

HO1	ATMR_CH0
LO1	ATMR_CH0N

HO2	ATMR_CH1
LO2	ATMR_CH1N
HO3	ATMR_CH2
LO3	ATMR_CH2N

Note: If PA0 and PA5 are not used as OPAMP output functions, they can serve as direct detection channels for the ADC. For specific configuration details, please refer to the description of ADC channel selection in the user manual.

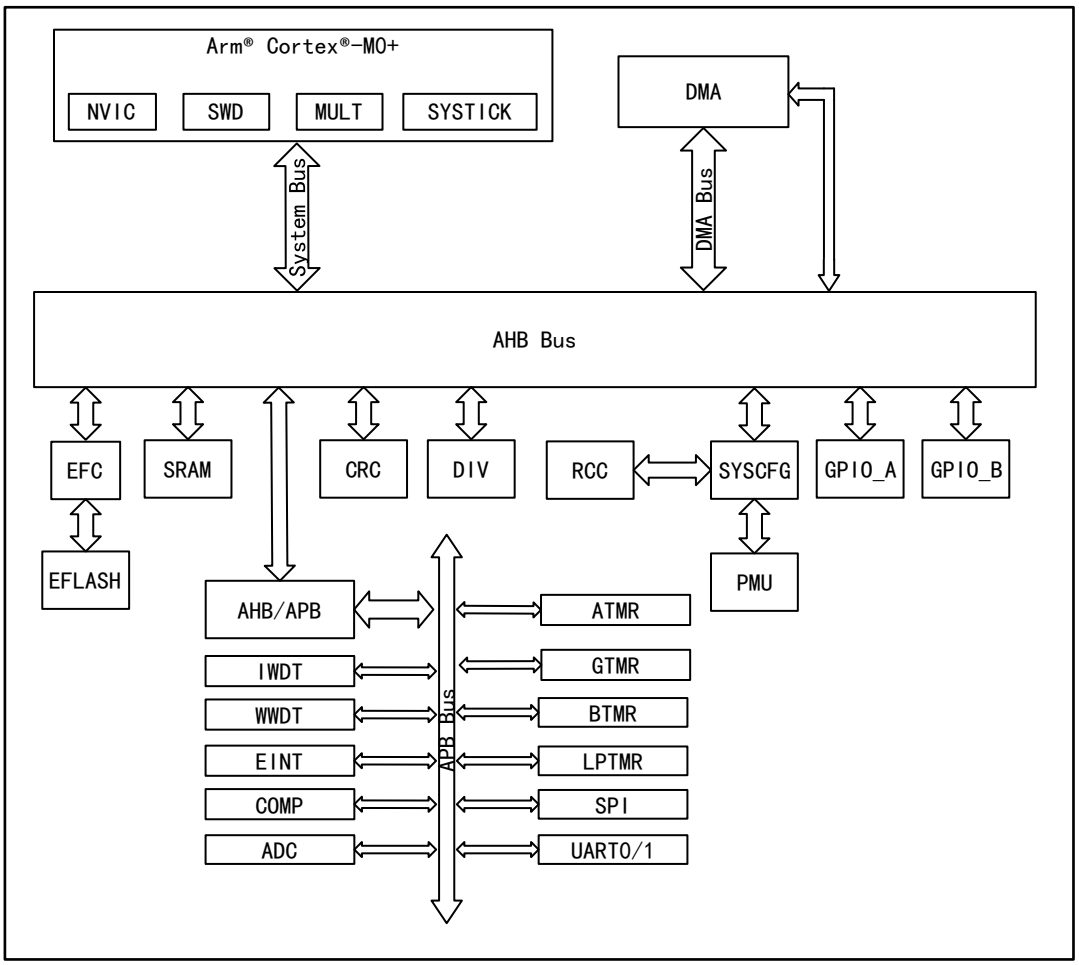
4 Functional Description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of G32M3101 series of products. For information about the Arm® Cortex®-M0+ core, refer to the *Arm® Cortex®-M0+ Technical Reference Manual*, which can be downloaded from Arm's website.

4.1 System Architecture

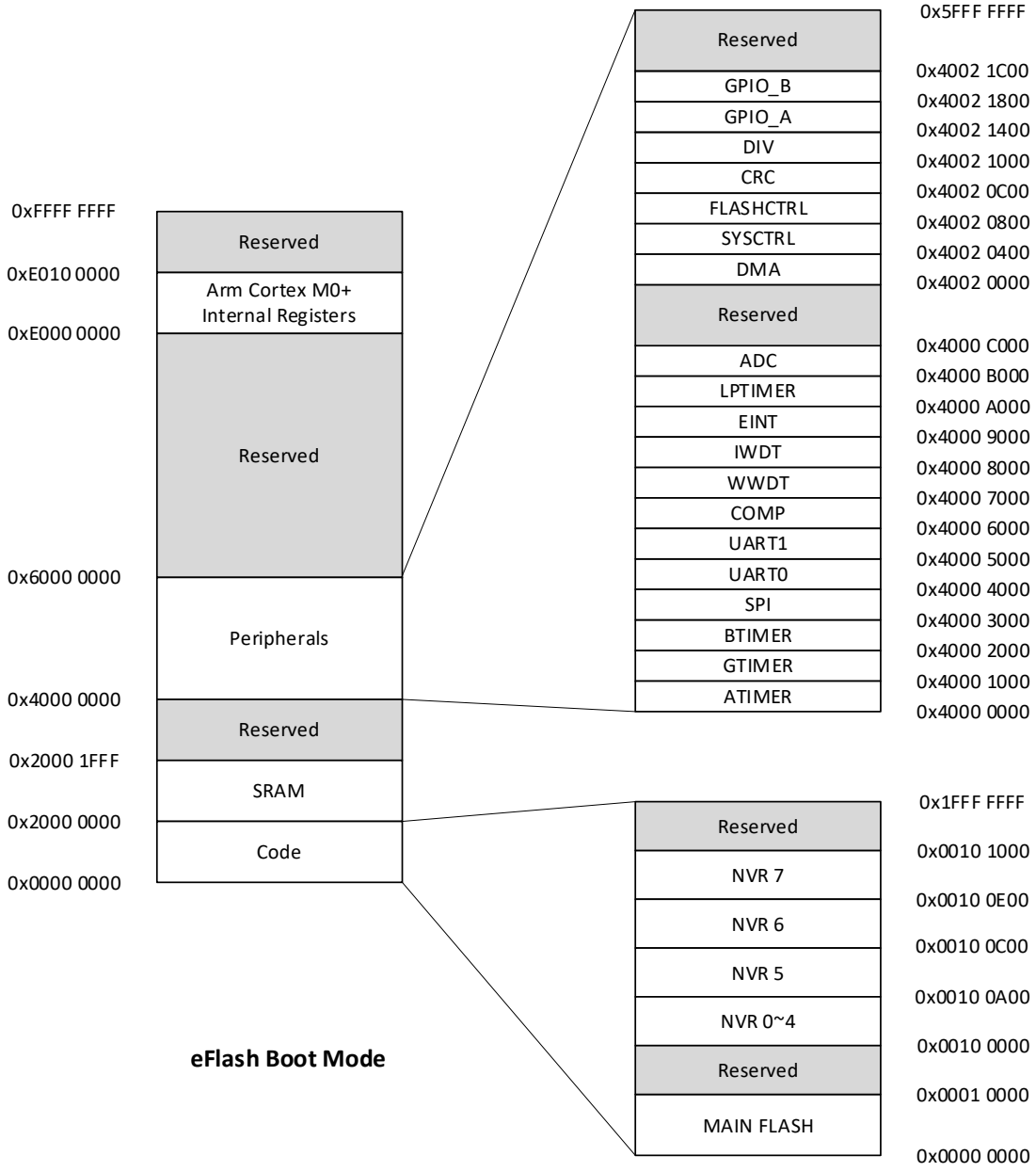
4.1.1 System Block Diagram

Figure 5 System Block Diagram



4.1.2 Address Mapping

Figure 6 Address Mapping



4.1.3 Start boot mode

The chip is activated by the Main memory (Main Flash). The main memory is mapped to the boot space, but it can still be accessed at its original address, that is, the contents of the flash memory can be accessed in two address areas.

4.2 Core

The core of G32M3101 is Arm® Cortex®-M0+, with its own MULT. based on a platform with low development cost, low power consumption, excellent computing performance and advanced system interrupt response. It is compatible with all Arm tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

1 built-in NVIC and it is capable of handling up to 32 maskable interrupt channels and 4 priority levels. It can pass the interrupt vector entry address directly to the core to achieve low-latency interrupt response processing to prioritize the late arrival of higher priority interrupts.

4.3.2 External Interrupt/Event Controller (EINT)

External interrupt/event controller has 28 edge detectors, each detector contains edge detection circuitry, interrupt/event request generation circuitry; each detector can be configured as a rising-edge triggered, falling-edge, double-edge triggered, but also able to individually mask. Up to 24 GPIOs can be connected to 14 external interrupt lines.

4.4 On-chip memory

The on-chip memory includes the main storage area, SRAM, and user area.

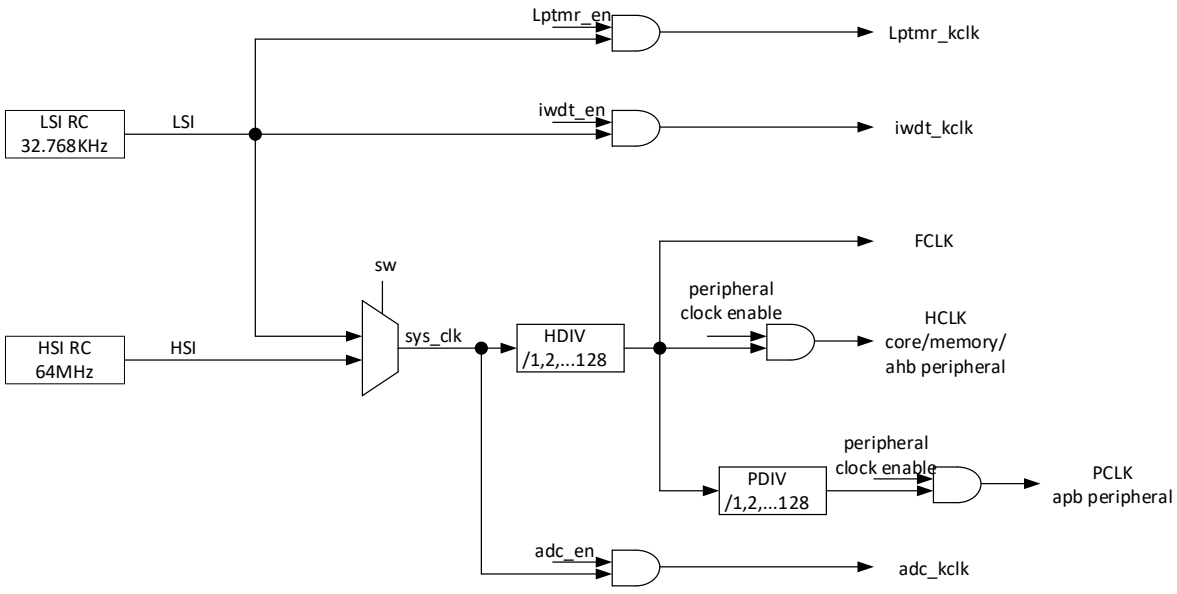
Table 7 On-chip Memory

Memory	Maximum Capacity	Function
Main memory area	64KB	Storage for user programme and data
SRAM	8 KB	CPU can access (read/write) with 0 cycles
User area	512 Bytes	Configuration of read/write protection of main memory area

4.5 Clock

4.5.1 Clock tree

Figure 7 Clock Tree



4.5.2 Clock sources

Clock source is divided into high-speed clock HSICLK and low-speed clock LSICLK according to the speed. In addition, some modules have additional clock source pins to obtain the required clock frequency through external circuits.

4.5.3 System clock

When the product is reset and started, HSICLK is started as the system clock by default, and if the interrupt is enabled, the software can receive the corresponding interrupt.

4.5.4 Bus clock

Built-in AHB, APB bus, the clock source of AHB is SYSCLK, and the clock source of APB is HCLK. Configure the dividing coefficient to obtain the required clock. The maximum frequency of AHB and APB is 64 MHz.

4.6 Power and power management

Note: The maximum rate is 1s/5V.

4.6.1 Power solution

Table 8 Power Supply Scheme

Name	Voltage range	Description
V_{BB}	5～36V	Supplies power to I/O (see pin diagram for specific I/O), and internal regulator through VBB pin.
V_{DD5}	5V	LDO reduces the input power supply voltage to 5V (VDD5) to power the internal analog modules of the chip.

Note: It is recommended to use 10uF and 100nF capacitors in parallel at the V_{BB} terminal, with a capacitor withstand voltage of no less than 50V. It is recommended to use 4.7uF, 100nF, and 5.6V clamping tubes in parallel at the VDD5 terminal.

4.6.2 Voltage regulator

Table 9 Regulator Operating Mode

Name	Description
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode

Note: The regulator is always in working state after reset.

4.6.3 Power supply voltage detector

Power-on reset (POR), power-down reset (PDR) are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit detects that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage detector (PVD) that monitors V_{BB} and

compares it to the V_{PVD} threshold, and generates an interrupt when VBB is outside of the V_{PVD} threshold range. The SoC can be set to a safe state through the interrupt service.

4.7 Low power mode

G32M3101 supports two low-power modes, which are sleep mode and stop mode. There are differences in power consumption, wake-up time and wake-up mode among these two modes. The low-power mode can be selected according to the actual requirements.

Table 10 Low Power Mode

Mode	Description
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the lowest power consumption can be achieved in stop mode. The clock of the internal 5V power supply stops. HSICLK is disabled, and LSICLK is enabled. The voltage regulator can be configured to normal mode or low-power mode. The SoC can be woken up by any external interrupt line, which consists of one of the 28 external interrupt lines, the PVD output.

4.8 DMA

A built-in DMA supports three DMA channels, each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, UART0/1, GTMR. Three levels of DMA channel priority can be configured, and data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

4.9 GPIO

The maximum driving capability of GPIO is 20mA. It can be configured as general input mode, general output mode, multiplexing function mode, and analog input and output mode. General-purpose input can be configured as high-impedance. General-purpose output can be configured as push-pull and open-drain output. Multiplexing functions can be used for digital peripherals. Analog input and output can be used for analog peripherals as well as for low-power modes. Pull-up/down resistors can be configured to enable/disable the pull-up/pull-down resistors. A maximum of 20MHz can be configured, and the higher the speed, the larger the power consumption and the higher the noise will be. Schmitt (Schmitt) inputs and non-Schmitt (CMOS) inputs are supported.

4.10 Communication peripherals

4.10.1 UART

Up to 2 built-in general-purpose asynchronous transceivers are supported, with the communication rate at 2.5Mbit/s. All UARTs can be configured with baud rate, parity bit, stop bit,

data bit length, and can support DMA. The functional differences of each UART are shown in the table below:

Table 11 UART Function Differences

UART Mode/Function	UART0	UART1
LIN mode	√	√
Standard features	√	√
Automatic baud rate detection	√	√
DMA	√	√
Receiver timeout interrupt	√	√
Oversampling rate	√	√

Note:√ means support.

4.10.2 SPI

1 built-in SPI, supports full-duplex and half-duplex communication in both master and slave modes. DMA controller can be used. Communication rate is 16~18Mbps.

4.11 Analog peripherals

4.11.1 ADC

1 built-in ADC with 12-bit accuracy, with up to 8+2 external channels and 6 internal channels. The internal channels measure the temperature sensor voltage and reference voltage, OPAMP0/1, 1/4VDD5 and 1/12VBB respectively. The A/D conversion modes of each channel are single, continuous or intermittent, and the ADC conversion results can be left-aligned or right-aligned stored in the data register. Segmented sampling is supported. DMA is supported.

4.11.1.1 Temperature sensor

1 built-in temperature sensor (TSensor), accuracy ±5℃. The voltage generated by the sensor varies linearly with the temperature, and can be converted to temperature by acquiring the converted voltage value from ADC.

Table 12 Tsensor Calibration Value

Calibration value name	Description	Address
V_{sensor_CAL}	Raw data collected at 25℃, V_{DD5}=5V	0x0010 0C14

4.11.1.2 Internal reference voltage

The internal reference voltage V_{BG} can be acquired by the ADC. V_{BG} provides a stable voltage output for the ADC.

Table 13 Calibration Value of Internal Reference Voltage

Calibration value name	Description	Address

V_{BG_CAL}	Raw data collected at 25℃(±5℃), V_{DD5}=5V(±10mV)	0x0010 0C1C

4.11.2 Comparator（COMP）

2 built-in fast rail-to-rail comparators, support internal/external reference voltage, hysteresis, rate, programmable function, and configurable output polarity. Reference voltage can be selected from external I/O, internal reference voltage (V_{BG}), internal reference voltage 1/4, 1/2 or 3/4. Interrupt can be generated. Support to wake up the SoC that are in sleep or stop mode through external interrupt.

4.11.3 Operational amplifier（OPAMP）

It is equipped with 2 rail-to-rail OPAMPs with magnification ratios of 1,4,6,8,10,12 and 16 times. The output mode can be selected, with built-in biases of 1/2 VDDA, 1/4 VDDA, BG or 1/4 BG.

4.12 Timer

1 built-in 16-bit advanced timer ATIMER, 1 32-bit general-purpose timer GTIMER, 1 16-bit basic timer BTIMER, 1 low-power timer LPTIMER,1 independent watchdog timer, 1 window watchdog timer, and 1 24-bit self-reducing system tick timer.

The watchdog timers can be used to check if a programme is running correctly.

The system tick timer is a peripheral of the core with an auto-reload function that generates a maskable system interrupt when the counter is 0. It can be used for a real-time operating system and time delay.

Table 14 Advanced/General/Basic/Low Power Timer Function Comparison

Item	Specific content/ Category	Advanced Timer	General Timer	Basic Timer	Low Power Consumption Timer
Name	-	ATIMER	GTIMER	BTIMER	LPTIMER
Time-based unit	Counter	16-bit	32-bit	16-bit	16-bit
	Prescaler	16-bit	16-bit	16-bit	16-bit
	Counting Mode	Up Down Center alignment	Up Down Center alignment	Up Down Center alignment	Up
Channel	Input Channel	0	4	3	0
	Capture Compare Channel	5	4	3	0
	Output channel	8	4	3	0
	Complementary output channel	3 groups	0	0	0
Function	Generate DMA request	No	Yes	No	No

Item	Specific content/ Category	Advanced Timer	General Timer	Basic Timer	Low Power Consumption Timer
	PWM mode	Yes	Yes	Yes	No
	Single pulse mode	Yes	Yes	Yes	No
	Forced output mode	Yes	Yes	Yes	No
	Deadband insertion	Yes	No	No	No

Table 15 IWDT and WWDT Comparison

Name	Counter resolution	Counter type	Prescaler factor	Function description
IWDT	12-bit	Down	Any integer between 1 and 256	The clock provided by an internal independent 32.768KHz RC oscillator. Because this RC oscillator is independent of the main clock, it can operate in stop modes. In case of problems, can reset the system. Can be used as a flexible timer to provide timeout management for applications.
WWDT	7-bit	Down	1/2/4/8	Can be set to run flexibly. In case of problems, can reset the system. Driven by the main clock with early warning interrupt function.

4.13 CRC

1 built-in CRC (Cyclic Redundancy Check) computing unit, which can generate CRC codes and can operate on 8-bit, 16-bit, and 32-bit data.

4.14 DIV

Include four 32-bit data registers that store divisor, dividend, quotient, and remainder respectively. It supports both signed and unsigned division.

4.15 Gate Driver

Integrated three-phase 36V gate driver capable of driving P/NMOS power transistors, integrated 5V LDO to provide power for the internal SoC. It is equipped with multiple built-in protection functions, including under-voltage protection. The under-voltage interrupt function (LVD) can be set, and the under-voltage flag bit is triggered when the VBB is lower than 3.4V. Input direct protection: When the inputs are of the same high or low, HO and LO will turn off the external P/NMOS power transistors. It also has a dead time of 240ns to effectively ensure the normal operation of the system. The four adjustable output slopes of HO/LO can be selected through system configuration.

5 Electrical Characteristics

5.1 Test Conditions of Electrical Characteristics

All voltage parameters (unless otherwise specified) refer to V_{SS}.

5.1.1 Maximum and Minimum Values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data obtained through comprehensive evaluation, design simulation or process characteristics are not tested on the production line. On the basis of comprehensive evaluation, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values after passing the sample test.

5.1.2 Typical values

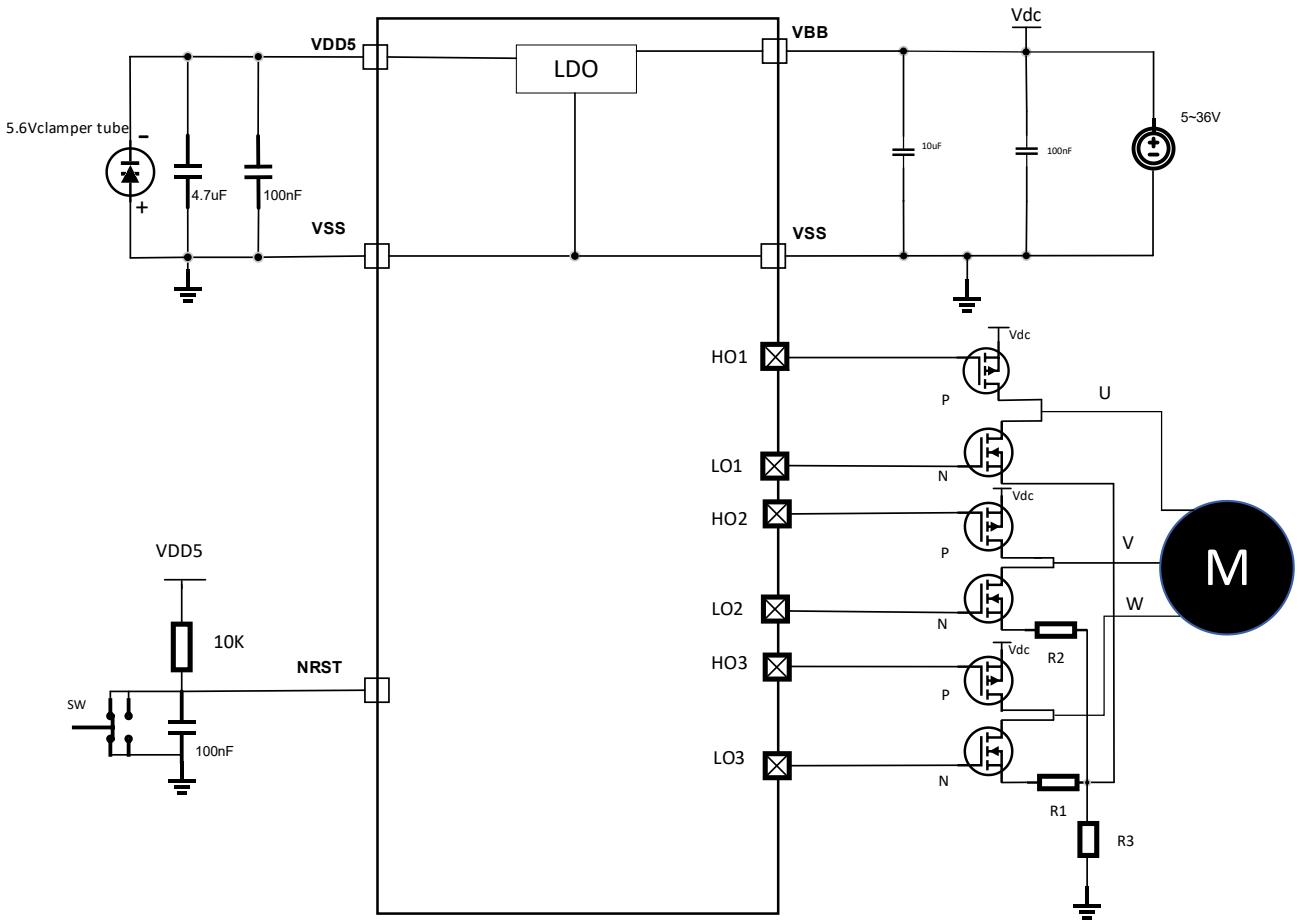
Unless otherwise specified, typical data are measured based on T_A=25℃, V_{BB}=36V. these data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves will not be tested on the production line, and will only be used for design guidance.

5.2 Typical application circuit diagram

Figure 8 Typical application circuit diagram



5.2.1 Load Capacitance

Figure 9 Load Conditions when Measuring Pin Parameters

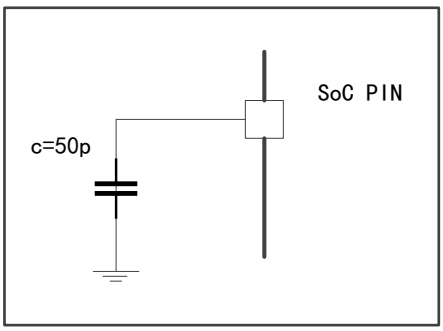


Figure 10 Pin Input Voltage Measurement Scheme

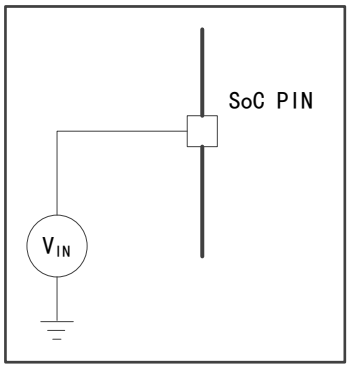
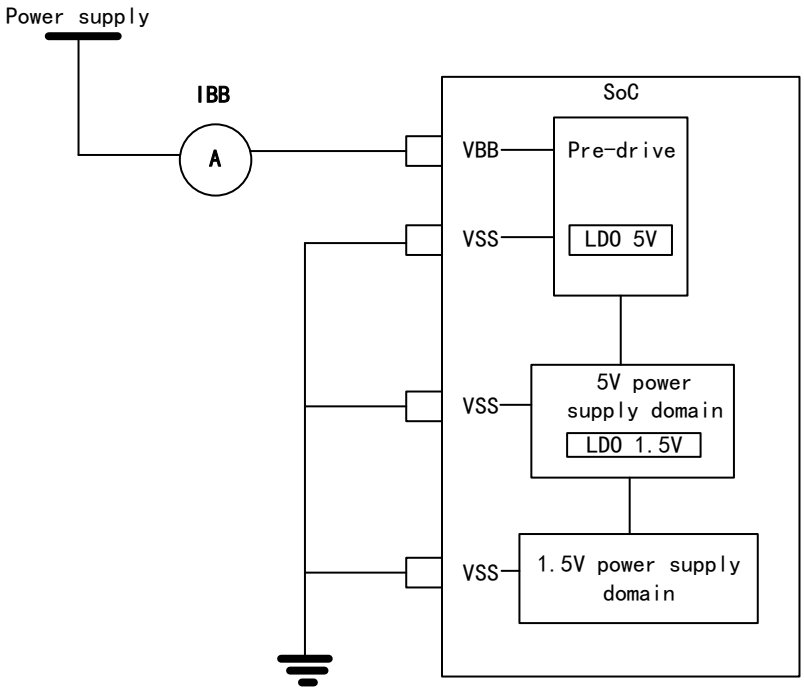


Figure 11 Power Consumption Measurement Scheme



5.3 Testing under General Working Conditions

Table 16 General Working Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	64	MHz
f_{PCLK}	Internal APB clock frequency	-	-	64	
V_{BB}	Power supply voltage input	-	5	36	V
V_{DD5}	SoC operating voltage	-	2.7	5.5	V

5.4 Absolute Maximum Rating

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage

to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.4.1 Maximum Temperature Characteristics

Table 17 Temperature Characteristics

Symbol	Description	Numerical value	Unit
T_{STG}	Storage temperature range	–65~150	℃
T_J	Maximum junction temperature	125	℃

5.4.2 Maximum Rated Voltage Characteristics

All power supply and ground pins must always be connected to the power supply within the external limited range.

Table 18 Maximum Rated Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{IN}	Input voltage on any other pin	-0.3	6	V
V_{BB}	Power supply voltage input	5	40	

5.4.3 Maximum Rated Current Characteristics

Table 19 Maximum Rated Current Characteristics

Symbol	Description	Max	Unit
ΣI_{VBB}	Total current into sum of all V_{BB} power lines (source)(1)	150	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	-150	
$I_{IO\ (PIN)}$	Output current sunk by any I/O and control pin	27	
	Output current source by any I/O and control pin	16	
$I_{INJ(PIN)}$	Injected current on NRST pins(2) (3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (other pins)(2) (4)	±10	

（1） All main power and ground pins must always be connected to the external power supply, in the permitted range.

（2） Forward/reverse injection current can interfere with the analog performance of the device.

（3） On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device.

（4） When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.4.4 ESD Characteristics

Table 20 ESD Characteristics

Symbol	Parameter	Condition	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (manikin)	T_A=+25℃, Standard: ANSI/ESDA/JEDEC JS-001-2017	4000	V

Symbol	Parameter	Condition	Max	Unit
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A=+25℃, Standard: ANSI/ESDA/JEDEC JS-001-2018	1000	

Note: It is tested by a third-party testing organization instead of in production.

5.4.5 Latch-up

Table 21 Latch-up

Symbol	Parameter	Condition	Max
LU	Class of static latch	T_A=105℃	150mA

Note: It is tested by a third-party testing organization instead of in production.

5.5 On-Chip Memory

5.5.1 Flash Characteristics

Table 22 Flash Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{prog}	32 bit programming time	T_A=-40~105℃，V_{BB}=36V	57	-	62	μs
t_{ERASE}	Page erase time		2.1	-	2.7	ms
t_{ME}	Whole erase time		30	-	32	ms
V_{prog}	Programming voltage	T_A=-40~105℃	2.7	-	5.5	V
t_{RET}	Data saving time	T_A =105℃	10	-	-	years
N_{RW}	Erase cycle	T_A=-40~105℃	100K	-	-	cycles

Note: It is tested in comprehensive evaluation instead of in production.

5.6 Clock System

5.6.1 Characteristics of Internal Clock Source

High speed internal (HSICLK)RC oscillator

Table 23 HSICLK Oscillator Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HSICLK}	Frequency	V_{BB}=3.5~ 36V,T_A=-40~105℃		-	64	-	MHz
$A_{CCHSICLK}$	Accuracy of HSICLK oscillat	Factory calibration	V_{BB}= 36V,T_A=25℃(1)	-1	-	1	%
			V_{BB}=3.5~ 36V,T_A=-40~105℃	-4.5	-	4.5	%
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{BB}=3.5V~ 36V,T_A=-40~105℃		10.8	-	12.6	μs
$I_{BB(HSICLK)}$	Power consumption of HSICLK oscillator			378	-	410	μA

Note: Except for (1) calibration in production, other data are obtained in comprehensive evaluation instead of in production.

Low speed internal (LSICLK)RC oscillator

Table 24 LSICLK Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSICLK}	Frequency	V_{BB}=3.5~36V,T_A=-40~105℃	31	32.768	34	KHz
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator		68	-	73	μs
Acc $_{(LSICLK)}$	-		-15	-	15	%
$I_{BB(LSICLK)}$	Power consumption of LSICLK oscillator		-	-	1	μA

Note: It is tested in comprehensive evaluation instead of in production.

5.7 Power Management

5.7.1 Power-on/power-down characteristics

Table 25 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{VBB}	V_{BB} rise time rate	-	0	-	200000	μs/V
	V_{BB} fall time rate		20	-	200000	

5.7.2 Characteristic test of embedded reset and power control module

Table 26 Embedded Reset and Power Control Module Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR5V}$(1)	Power-on/power-down reset threshold	Falling edge	2.1	2.4	2.6	V
		Rising edge	2.3	2.5	2.7	V
$V_{PDRhyst5V}$	5V PDR hysteresis	-	0.1	-	0.2	V
T_{RST5V}	Reset duration	-	70	120	300	μs
$V_{POR/PDR1.5V}$(1)	Power-on/power-down reset threshold	Falling edge	1.15	1.2	1.25	V
		Rising edge	1.25	1.3	1.35	V
$V_{PDRhyst1.5V}$	1.5V PDR hysteresis	-	0.1	-	0.2	V
$T_{RST1.5V}$	Reset duration	-	70	120	300	μs

Note: It is tested in comprehensive evaluation instead of in production.

（1）PDR detector monitors V_{BB} and V_{DDA} (if enabled in option byte), POR detector monitors V_{BB} only.

Table 27 Programmable Voltage Detector Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD5V}	Level selection of programmable voltage detector	PLS[2:0]=000 (rising edge)	2.70	-	2.74	V
		PLS[2:0]=000 (falling edge)	2.61	-	2.67	V
		PLS[2:0]=001 (rising edge)	2.99	-	3.04	V
		PLS[2:0]=001 (falling edge)	2.90	-	2.96	V
		PLS[2:0]=010 (rising edge)	3.31	-	3.36	V
		PLS[2:0]=010 (falling edge)	3.20	-	3.27	V
		PLS[2:0]=011 (rising edge)	3.59	-	3.66	V
		PLS[2:0]=011 (falling edge)	3.50	-	3.57	V
		PLS[2:0]=100 (rising edge)	3.90	-	3.96	V
		PLS[2:0]=100 (falling edge)	3.81	-	3.90	V
		PLS[2:0]=101 (rising edge)	4.19	-	4.27	V
		PLS[2:0]=101 (falling edge)	4.10	-	4.19	V
		PLS[2:0]=110 (rising edge)	4.49	-	4.57	V
		PLS[2:0]=110 (falling edge)	4.39	-	4.49	V
		PLS[2:0]=111 (rising edge)	4.74	-	4.84	V
		PLS[2:0]=111 (falling edge)	4.67	-	4.78	V
$V_{PVDhyst5V}$	PVD hysteresis	-	-	100	-	mV

Note: It is tested in comprehensive evaluation instead of in production.

5.7.3 BG

Table 28 BG characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBG	BG voltage	V_{BB}=36V，T_A=-40~105℃	1.22	-	1.25	V
Ibias	BG current		0.95	-	1.1	uA

5.7.4 LDO5V

Table 29 LDO5V characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
-	current-limiting protection	V_{BB}=36V，T_A=-40~105℃	73	-	105	mA
V_{LDO5}	LDO5 voltage		4.98	-	5.06	V

5.8 Power Consumption

5.8.1 Power consumption test environment

(1) Test under the conditions of Coremark, KeilV5 compiling environment and L3 compiling optimization level.

(2) All I/O pins are configured as analog inputs, which are connected to VBB or V_{SS} (non-load) at a static level.

(3) Unless otherwise specified, all peripherals are turned off.

(4) The relationship between the setting of flash waiting period and f_{HCLK}:

0~16MHz: 0 waiting periods,

16~32MHz: 1 waiting periods,

32~64MHz: 2 waiting periods.

(5) Instruction prefetch function is enabled (Note: this bit must be set before clock setting and bus frequency division).

5.8.2 Running mode

Table 30 The program is executed in Flash, and the power consumption in running mode

Parameter	Condition	f_{HCLK}	T_A=25℃, V_{BB}=6.4V	T_A=105℃, V_{BB}=36V
			Typ	Max
			I_{BB}(mA)	I_{BB}(mA)
Power consumption in running mode	HSECLK bypass, enabling all peripherals	64MHz	5.24	5.25
		32MHz	3.35	3.23
		16MHz	2.53	2.71
		8MHz	2.11	2.21
	HSECLK bypass, turn off all peripherals	64MHz	2.63	3.50
		32MHz	2.49	2.51
		16MHz	2.07	2.22
		8MHz	1.85	1.93

Note: It is tested in comprehensive evaluation instead of in production.

Table 31 Power Consumption in Sleep mode when the program is executed in Flash

Parameter	Condition	f_{HCLK}	T_A=25℃, V_{BB}=6.4V	T_A=105℃, V_{BB}=36V
			Typ	Max
			I_{BB}(mA)	I_{BB}(mA)
Power consumption in sleep mode	HSECLK bypass, enabling all peripherals	64MHz	2.63	3.73
		32MHz	2.39	2.61
		16MHz	1.85	2.04
		8MHz	1.60	1.76

Parameter	Condition	f_{HCLK}	T_A=25℃, V_{BB}=6.4V	T_A=105℃, V_{BB}=36V
			Typ	Max
			I_{BB}(mA)	I_{BB}(mA)
	HSECLK bypass, turn off all peripherals	64MHz	1.82	2.02
		32MHz	1.53	1.72
		16MHz	1.37	1.56
		8MHz	1.31	1.48

Notes: It is tested in comprehensive evaluation instead of in production.

Table 32 Power Consumption in stop mode

Parameter	Condition	Typ	Max	Unit
		T_A=25℃, V_{BB}=6.4V	T_A=105℃, V_{BB}=36V	
Power Consumption in stop mode	The kernel and most peripheral devices stop running, while IO, SRAM, and registers remain. The voltage regulator is in low-power mode. HSI is off and LSI is on.	147.83	175	μA

Notes: It is tested in comprehensive evaluation instead of in production.

5.9 Wake-up Time in Low Power Mode

The measurement of wake-up time with low power consumption is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{BB}=V_{DDA}.

Table 33 Low Power Wake-up Time

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{WUSLEEP}$	Wake up from sleep mode	V_{BB}=36V, T_A=-40~105℃	-	1	-	μs
t_{WUSTOP}	Wake up from stop mode		-	34	-	

Note: It is tested in comprehensive evaluation instead of in production.

5.10 I/O Port Characteristics

Table 34 DC Characteristics (T_A=-40℃-105℃,V_{BB}=6.4V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	-	-	-	0.3V_{DD5}	V
V_{IH}	Input high level voltage	-	0.7V_{DD5}	-	-	V
V_{hys}	Schmitt trigger hysteresis	-	0.07V_{DD5}	-	-	V
I_{lkg}	Input leakage current	V_{SS}≤V_{IN}≤V_{DDIOx}	-	-	1	μA
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	V_{IN}=V_{DDIOx}	30	40	50	kΩ

Table 35 AC Characteristics (T_A =25℃)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{max(IO)out}$	Maximum frequency	C_L=25pF，16MHz， V_{DD5}=5V，T_A=-40~105℃	-	-	16	MHz
$t_{f(IO)out}$	Output falling time from high to low level		2.2	-	3.7	ns
$t_{r(IO)out}$	Output rising time from low to high level		3.2	-	8.8	ns

Figure 12 Definition of Input and Output AC characteristics

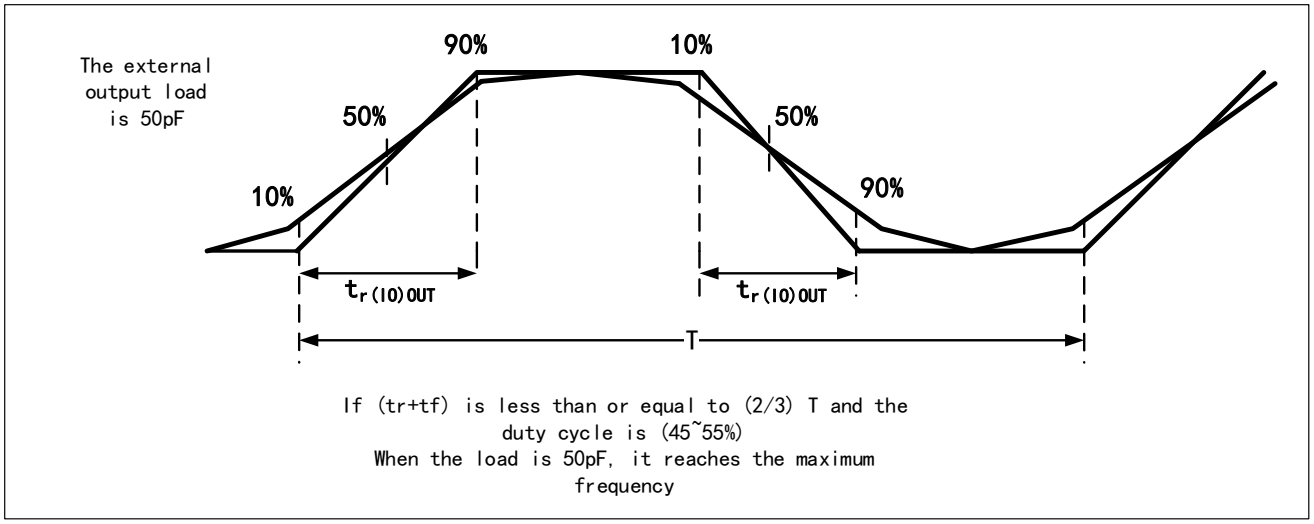


Table 36 Output Drive Current Characteristics (T_A =25℃)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=10mA, V_{DDIOx}≥2.7V	-	-	0.4	V
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-0.4	-	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=20mA, V_{DDIOx}≥2.7V	-	-	0.4	
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-0.4	-	-	

Note: It is tested in comprehensive evaluation instead of in production.

5.11 NRST pin characteristics

The input drive of NRST pin adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}

Table 37 NRST Pin Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low voltage	V_{BB}=3.5~36V,T_A=-40~105℃	2.16	-	3.08	V
$V_{IH(NRST)}$	NRST input high voltage		1.48	-	2.24	
$V_{hys(NRST)}$	Voltage hysteresis of NRST Schmitt trigger		680	-	880	mV
R_{PU}	Weak pull-up equivalent resistance		37	-	58	kΩ

5.12 Communication Interface

5.12.1 SPI Interface Characteristics

Table 38 SPI Characteristics (T_A=25℃, V_{DD5}=5V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	-	MHz
		Slave mode	-	16	-	
$t_{r(SCK)}$	SPI clock rising time	Master mode	4.5	-	5.0	ns
$t_{f(SCK)}$	SPI clock falling time		3.5	-	4	
$t_{su(NSS)}$	NSS setup time	Slave mode	$4T_{PCLK}$	-	36.8	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2T_{PCLK}$ + 10	-	50.1	ns
$t_{w(SCKH)}$	SCK high time	Master mode	25.9	-	26.2	ns
$t_{w(SCKL)}$	SCK low time		27.4	-	28.5	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	13.9	-	16.1	ns
		Slave mode	25.1	-	58.2	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	38.2	-	39.4	ns
		Slave mode	28.3	-	30.1	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK}=20MHz	49.5	-	51.1	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	41.7	-	45.2	ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	13.1	-	15.8	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	16.9	-	21.0	ns
$t_{h(SO)}$	Data output holding time	Slave mode (after enable edge)	13.3	-	14.6	ns
$t_{h(MO)}$		Master mode (after enable edge)	13.4	-	13.7	

Note: It is tested in comprehensive evaluation instead of in production.

Figure 13 SPI Timing Diagram—Slave Mode and CPHA=0

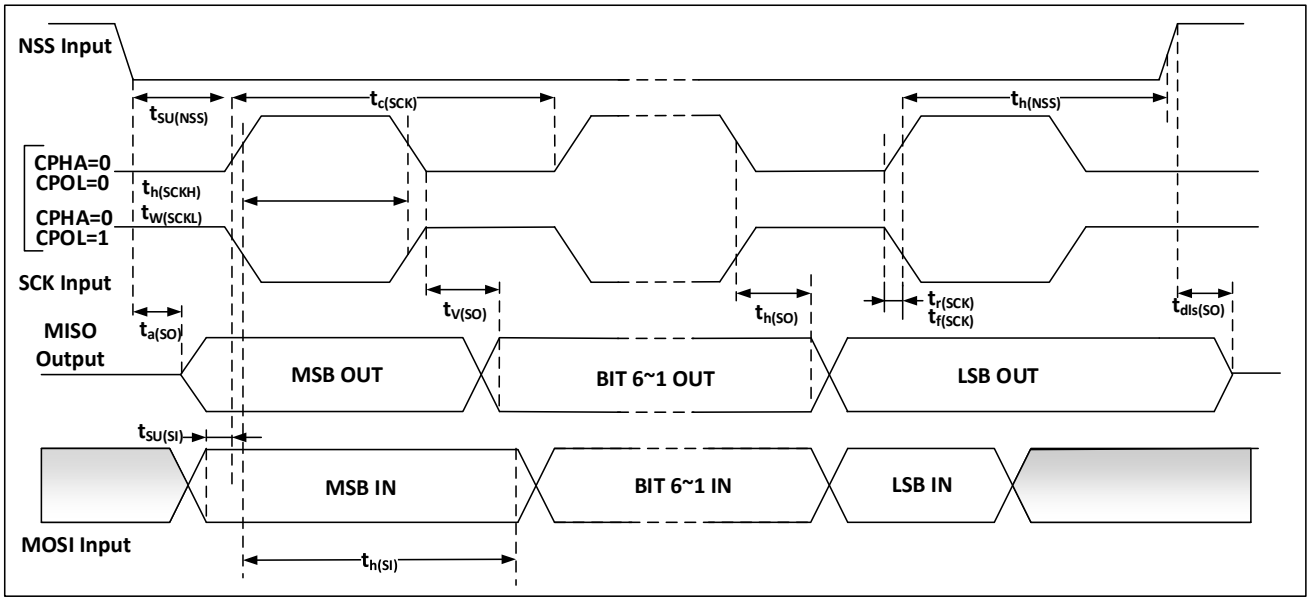
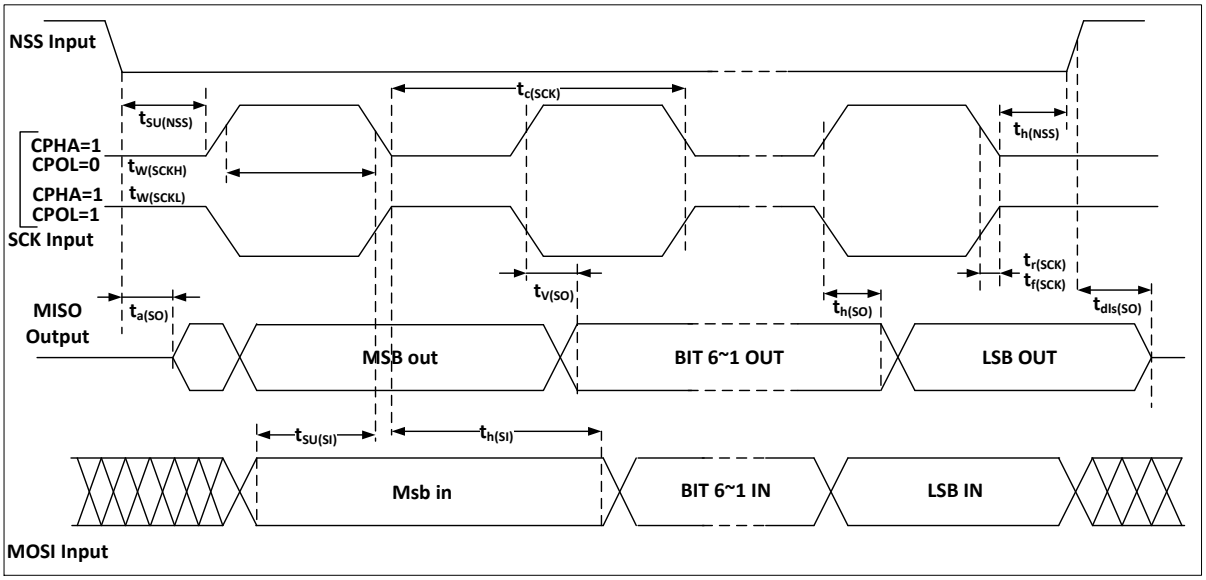
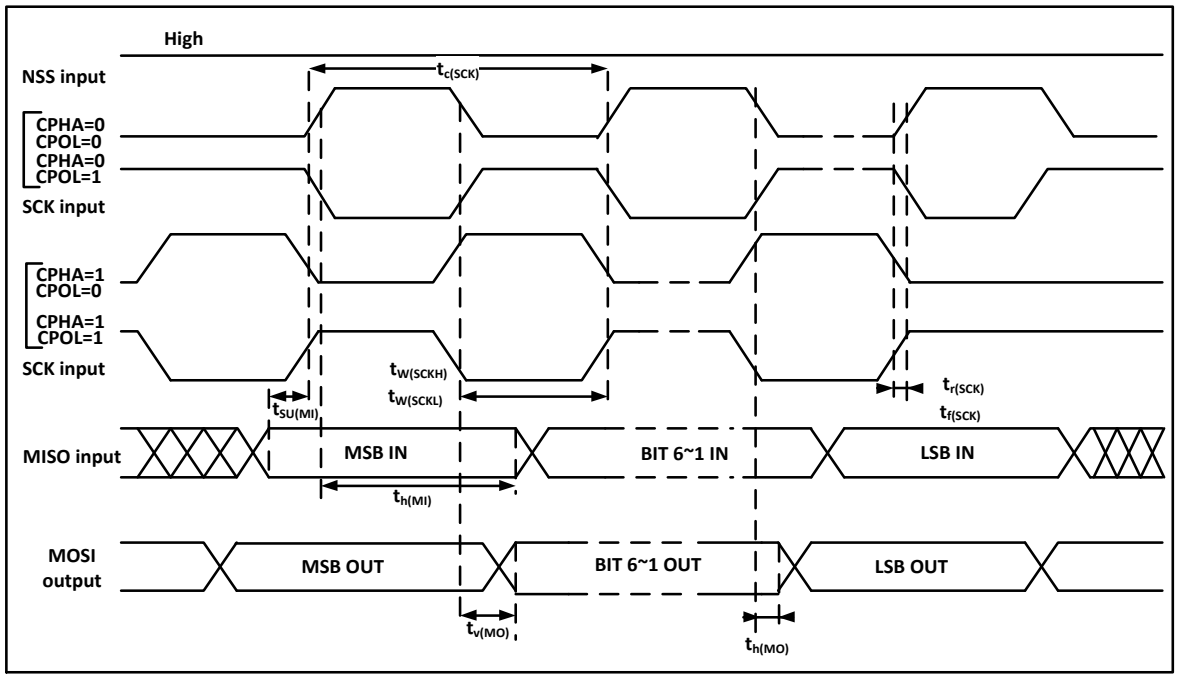


Figure 14 SPI Timing Diagram —Slave Mode and CPHA=1



Note: the measuring points are set at CMOS levels: $0.3V_{DD5}$ and $0.7V_{DD5}$.

Figure 15 SPI Timing Diagram—Master mode



Note: the measuring points are set at CMOS levels: $0.3V_{DD5}$ and $0.7V_{DD5}$.

5.13 ADC

5.13.1 12-bit ADC Characteristics

Table 39 12-bit ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	supply voltage	-	2.7	-	VDD5	V
I_{DDA}	ADC power consumption	V_{BB}=36V T_A=-40/25/105℃	2.29	-	2.47	mA
f_{ADC}	ADC frequency	V_{DDA}=2.7~VDD5	0.6	16	32	MHz
C_{ADC}	Internal sample and hold capacitor	-	-	5.5	-	pF
R_{ADC}	Sampling resistance	-	-	-	1000	Ω
T_{CONV}	Sampling and conversion time	f_{ADC}=32MHz,12-bit convert, V_{BB}=36V T_A=-40/25/105℃	0.8	-	8.7	μs
Fs	-	-	-	-	2	msPS

Note: It is tested in comprehensive evaluation instead of in production.

Table 40 Accuracy of 12-bit ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$\|E_T\|$	Composite error	V_{BB}=36V Vref=5V Extracorporeal perfusion T_A=-40/25/105℃	0	-	5	LSB
$\|E_O\|$	Offset error		0	2	3.5	
$\|E_G\|$	Gain error		0	3	5	

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$\|E_D\|$	Differential linear error		0	1	1.5	
$\|E_L\|$	Integral linearity error		0	1.5	2.5	

Note: It is tested in comprehensive evaluation instead of in production.

5.13.2 Temperature Sensor Characteristics

Table 41 Temperature Sensor Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Slope	Average slope	V_{BB} = 36V, T_A = -40~105℃, Vref=5V	-	4.3	-	mV/ºC
Tsline			-1	-	3.1	℃
Tssample_25℃	-	V_{BB} =36V, T_A =25℃, Vref=5V	-	1170	-	mV

5.14 Comparator

Table 42 Comparator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.7	5	5.5	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}-0.05	V
V_{OUT}	Comparator output voltage range	-	0	-	V_{DDA}	V
t_D	propagation delay	Input amplitude 0~V_{DD5}, rising edge	50	-	62	ns
		Input amplitude 0~V_{DD5}, falling edge	46	-	63	
-	Operating current	T_A=-40~105℃/ V_{BB}=36V	40	-	70	μA
-	Offset voltage	-	-3.2	-	5.5	mV

Note: It is tested in comprehensive evaluation instead of in production.

5.15 Operational amplifier

Table 43 Operational amplifier Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDDA	Analog power supply voltage	-	4	5	5.5	V
CMIR	Common-mode input range	T_A=-40~105℃/ V_{BB}=36V	0	-	V_{DDA}/2	V
Voffset	Input offset voltage		-1.3	-	2.7	mV
IDDOPAMP	Current consumption		1.95	-	2.53	mA
SR	Slew rate	rising edge	49.3	-	73.0	V/μs
		falling edge	19.9	-	28.9	
Twakeup		T_A=-40~105℃/ V_{cm}=0.5VDDA	0.35	-	5.84	us

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Setup time from shutdown to wake-up	T_A=-40~105℃/ V_{cm}=0.25VBG	0.32	-	0.39	us
VOHSAT	High saturation output voltage	T_A=-40~105℃/ V_{BB}=36V	V_{DDA}-0.05	-	V_{DDA}	V
VOLSAT	Low saturation output voltage		2.10	-	3.61	mV
-	Absolute gain accuracy error		0.22	-	1.3	%
-	Relative gain accuracy error		-0.06	-	0.41	

Note: It is tested in comprehensive evaluation instead of in production.

5.16 Gate Driver

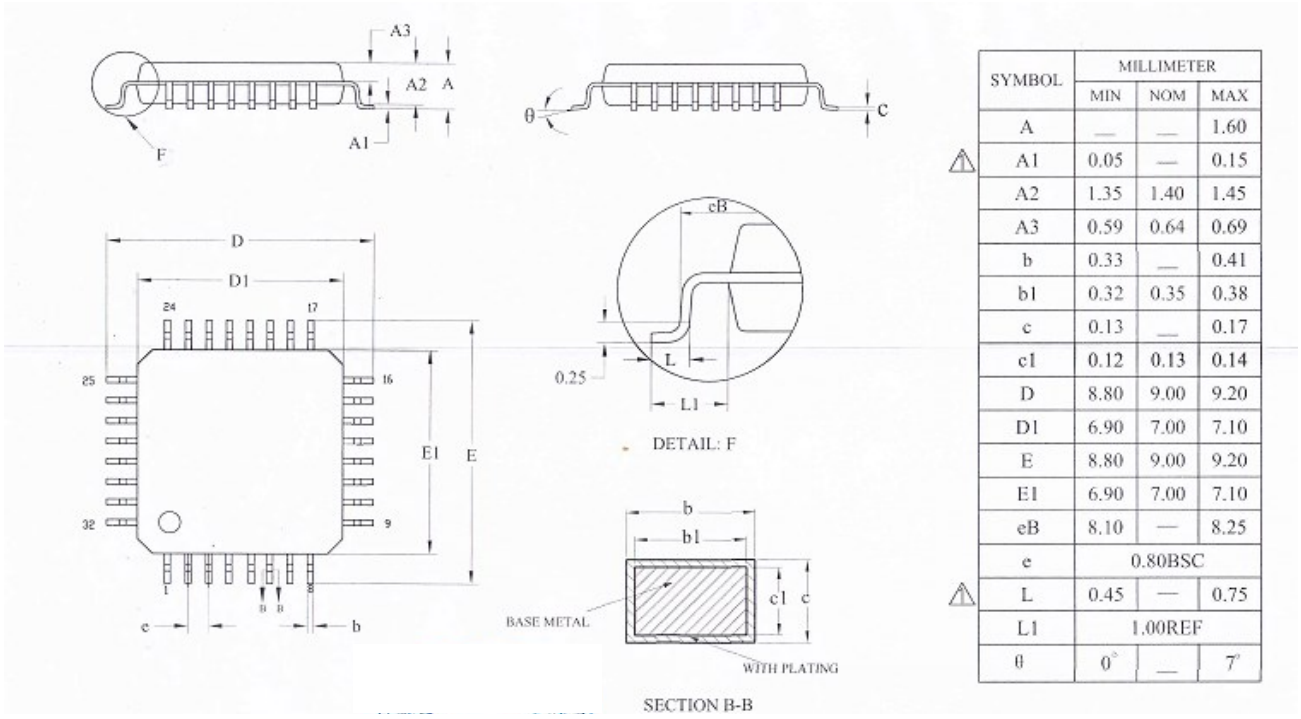
Table 44 Gate Driver Characteristics

Parameter	Condition	Min	Typ	Max	Unit
VBB under-voltage high level potential	T_A=-40~105℃/V_{BB}=36	3.5	-	3.66	mA
VBB under-voltage low level potential		3.26	-	3.41	V
VBB under-voltage hysteresis potential		0.21	-	0.26	V
HO output current		272	-	334	mA
HO input current		72	-	98	mA
LO output current		74	-	92	mA
LO input current		174	-	234	mA
HO output voltage		13.2	-	13.6	V
LO output voltage		10.4	-	11	V
HO output rise time (470pF)	PREDRV_HO_RISE_SEL=00	124	-	164	ns
	PREDRV_HO_RISE_SEL=01	76	-	104	ns
	PREDRV_HO_RISE_SEL=10	49	-	64	ns
	PREDRV_HO_RISE_SEL=11	42	-	54	ns
HO output fall time (470pF)	PREDRV_HO_FALL_SEL=00	546	-	716	ns
	PREDRV_HO_FALL_SEL=01	296	-	408	ns
	PREDRV_HO_FALL_SEL=10	176	-	240	ns
	PREDRV_HO_FALL_SEL=11	144	-	208	ns
LO output rise time (470pF)	PREDRV_LO_RISE_SEL=00	748	-	997	ns
	PREDRV_LO_RISE_SEL=01	392	-	516	ns
	PREDRV_LO_RISE_SEL=10	238	-	340	ns
	PREDRV_LO_RISE_SEL=11	202	-	316	ns
LO output fall time (470pF)	PREDRV_LO_FALL_SEL=00	136	-	184	ns
	PREDRV_LO_FALL_SEL=01	92	-	124	ns
	PREDRV_LO_FALL_SEL=10	66	-	88	ns
	PREDRV_LO_FALL_SEL=11	56	-	80	ns
Deadband time (empty load)	DTH-L	213	-	230	ns
	DTL-H	210	-	226	ns
Matching time for high and low sides	MTΔTon	-	-	30	ns
	MTΔToff	-	-	30	ns

6 Package Information

6.1 LQFP32 Package Information

Figure 16 LQFP32 Package Diagram

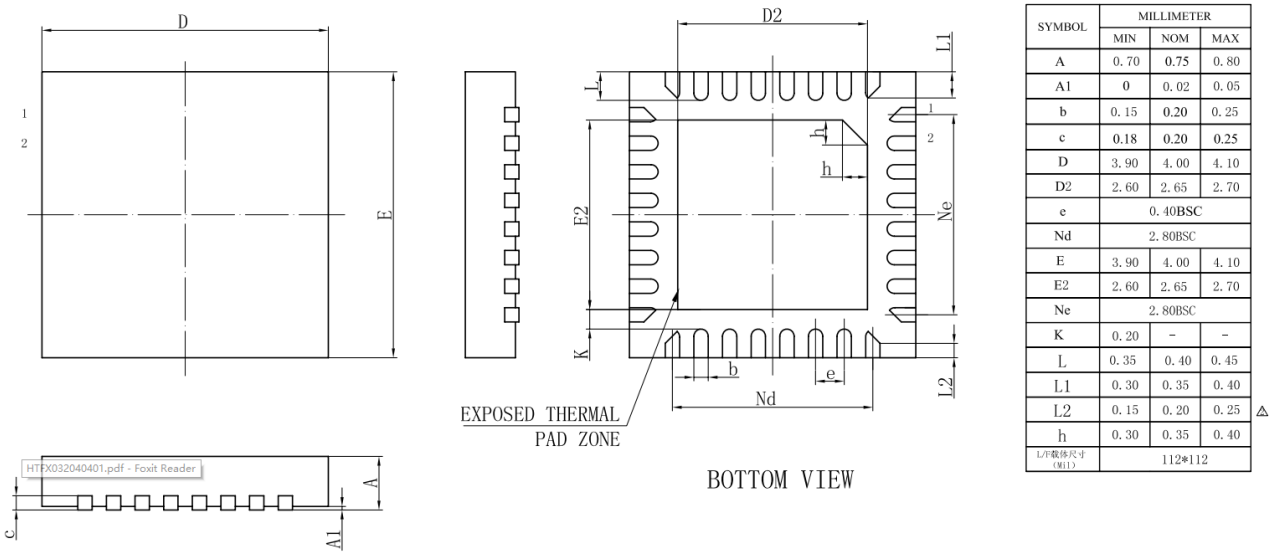


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.80BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0°	—	7°

Note: The figure is not drawn to scale.

6.2 QFN32 Package Information

Figure 17 QFN32 Package Diagram

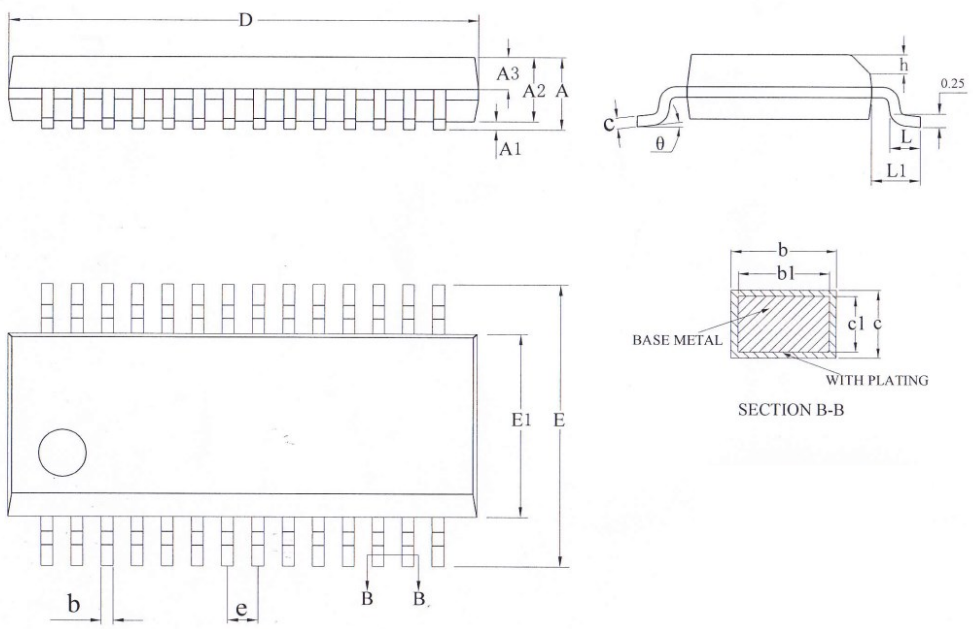


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸 (M11)	112*112		

Note:The figure is not drawn to scale.

6.3 SSOP28 Package Information

Figure 18 SSOP28 Package Diagram

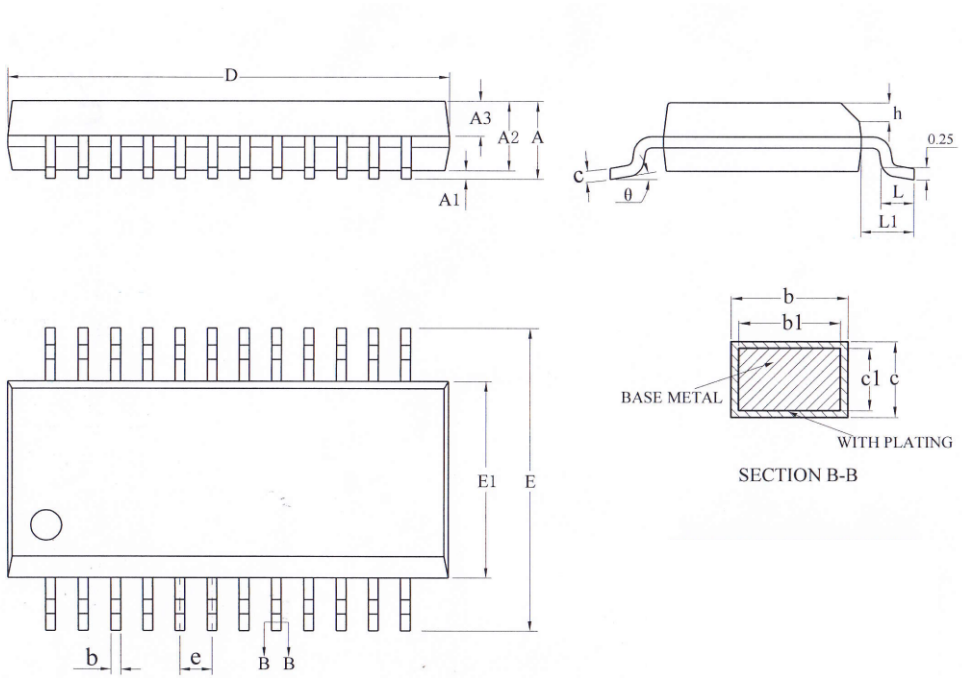


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0°	—	8°

Note:The figure is not drawn to scale.

6.4 SSOP24 Package Information

Figure 19 SSOP24 Package Diagram



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Note:The figure is not drawn to scale.

6.5 Package Designator

Figure 20 LQFP Package Designator

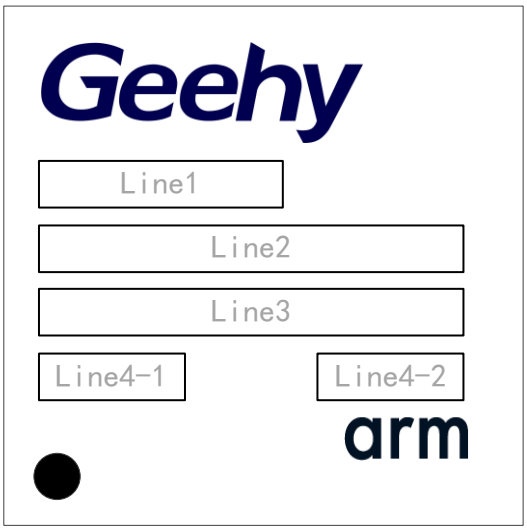


Table 45 LQFP silk-screen printing figure description

Symbols and Icons	description
Geehy	Geehy
Line1	Product Series
Line2	product model
Line3	batch number
Line4-1	Internal traceability code
Line4-2	Year and week number
arm	Arm authorization identification
●	PIN1 location

Note: The number of digits in each column above is not fixed.

Figure 21 QFN Package Designator

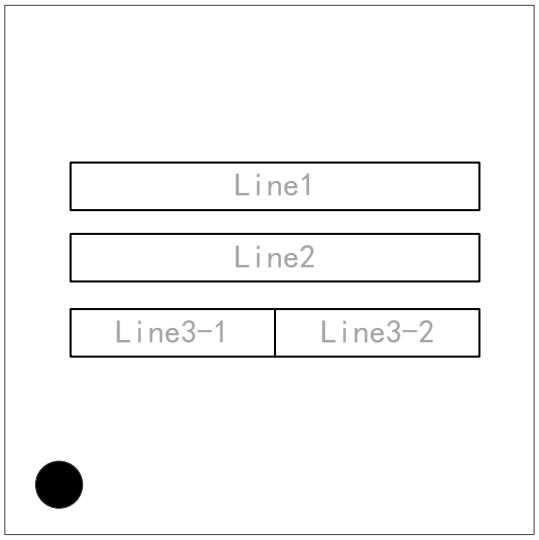


Table 46 QFN silk-screen printing figure description

Symbols and Icons	description
Line1	product model
Line2	batch number
Line3-1	Internal traceability code
Line3-2	Year and week number
●	PIN1 location

Note: The number of digits in each column above is not fixed.

Figure 22 SSOP Package Designator

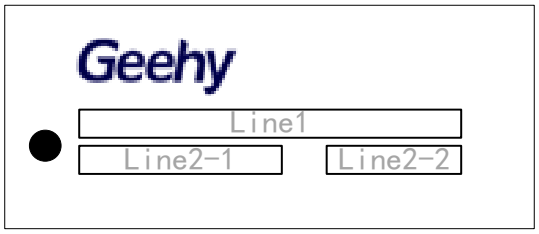


Table 47 SSOP silk-screen printing figure description

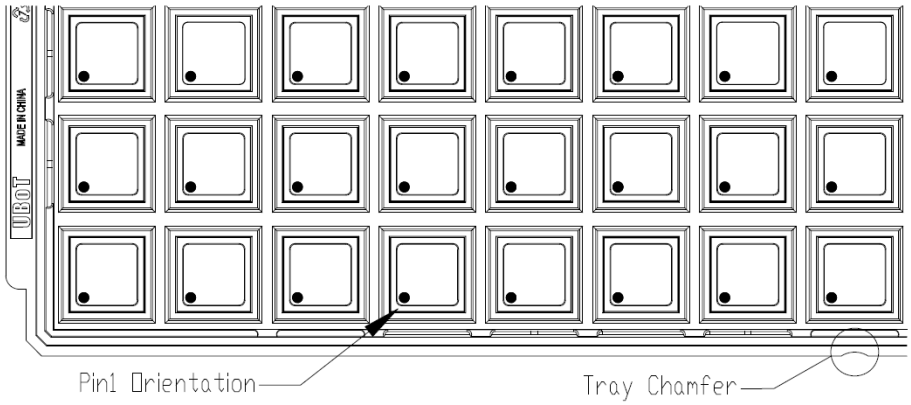
Symbols and Icons	description
Geehy	Geehy
Line1	product model
Line2-1	batch number
Line2-2	Year and week number
●	PIN1 location

Note: The number of digits in each column above is not fixed.

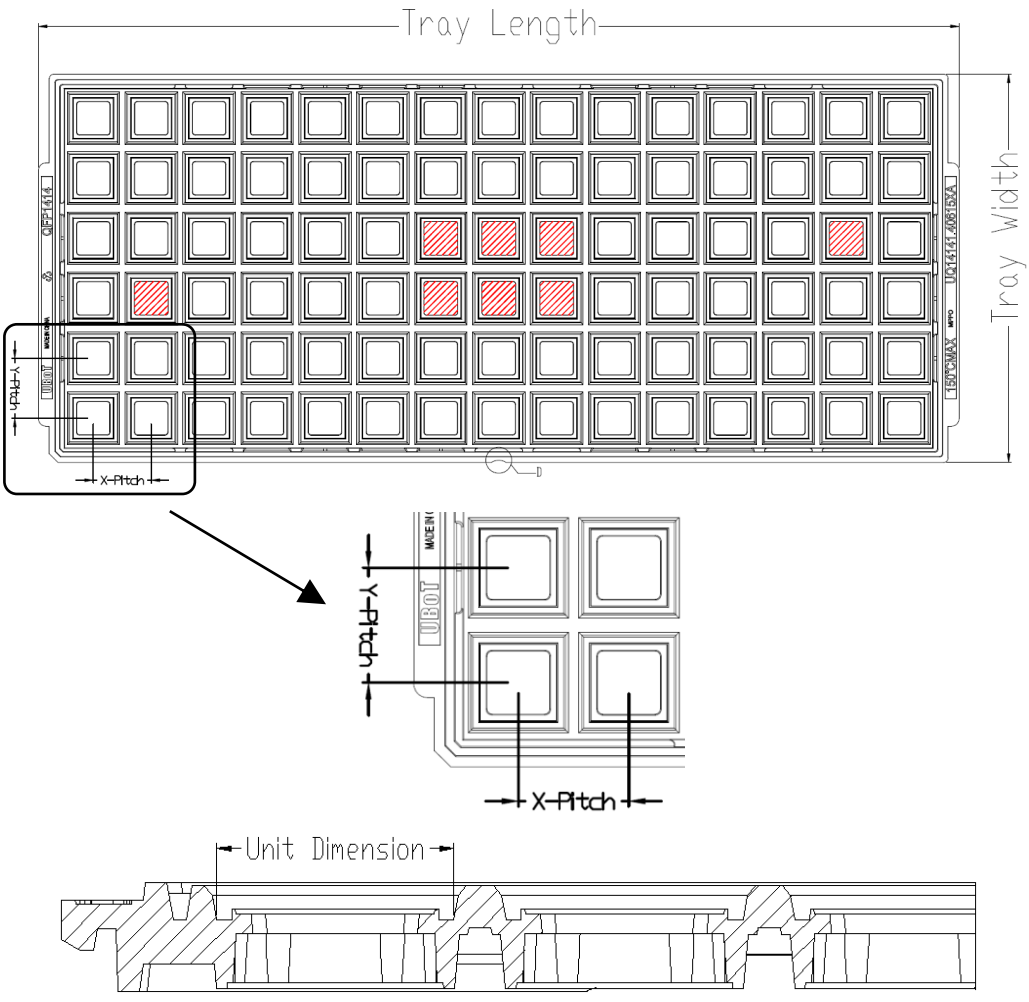
7 Packaging Information

7.1 Tray packaging

Figure 23 Tray Packaging Diagram



Tray Dimensions



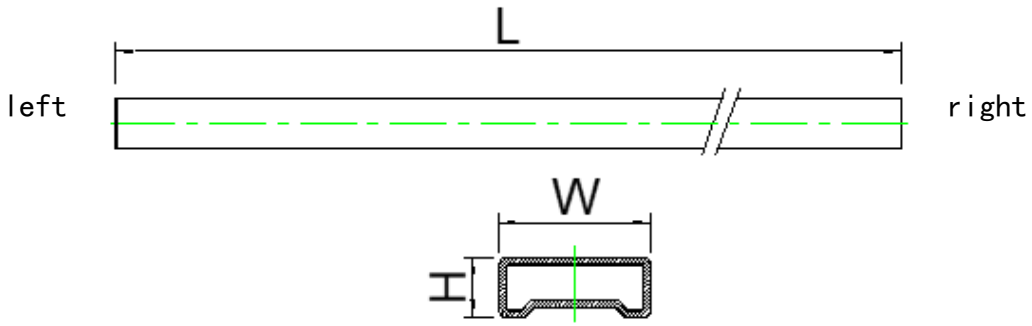
Note: All photos are for reference only, and the appearance is subject to the product

Table 48 Parameter Specification Table of Pallet Packaging

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
G32M3101K8T6	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32M3101K8U6	QFN	32	4900	4.185	4.185	8.8	9.2	322.6	135.9
G32M3101K8T7	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32M3101K8U7	QFN	32	4900	4.185	4.185	8.8	9.2	322.6	135.9

7.2 Tube packaging

Figure 24 Tube package drawing



Note: All photos are for reference only, and the appearance is subject to the product.

Table 49 Specification table of tube packaging parameters

Device	Package Type	Pins	SPQ	L(mm)	W(mm)	H(mm)
G32M3101G8S6	SSOP	28	5000	520	7.8	3.4
G32M3101E8S6	SSOP	24	5000	520	7.8	3.4
G32M3101G8S7	SSOP	28	5000	520	7.8	3.4
G32M3101E8S7	SSOP	24	5000	520	7.8	3.4

Note: SPQ= Smallest Package Quantity.

8 Ordering Information

Table 50 Product naming definition

product name			
G32M3101K8T6			
name Example	definition	name	information
G32	Product Series	G32	Arm -based 32-bit SoC
M	Product type	M	Electrical machinery
31	Product subseries	3x	General
0	Driver type	0	PN Die
1	Driver voltage endurance	1	0~40V
G	Number of pins	E	24 pins
		G	28 pins
		K	32 pins
8	Flash memory capacity	8	64KB
T	Package	T	LQFP
		U	QFN
		S	SSOP
6	Temperature range	6	temperature range:-40℃~85℃
		7	temperature range:-40℃~105℃
T	pack	Blank	Tray packaging
		T	Tube packaging

Table 51 Ordering Information List

Order Code	FLASH（KB）	SRAM（KB）	Package	SPQ	Temperature range
G32M3101K8T6	64	8	LQFP32	2500	-40℃~85℃
G32M3101K8U6	64	8	QFN32	4900	-40℃~85℃
G32M3101G8S6-T	64	8	SSOP28	5000	-40℃~85℃
G32M3101E8S6-T	64	8	SSOP24	5000	-40℃~85℃
G32M3101K8T7	64	8	LQFP32	2500	-40℃~105℃
G32M3101K8U7	64	8	QFN32	4900	-40℃~105℃
G32M3101G8S7-T	64	8	SSOP28	5000	-40℃~105℃
G32M3101E8S7-T	64	8	SSOP24	5000	-40℃~105℃

9 Commonly Used Function Module Denomination

Table 52 Commonly Used Function Module Denomination

Full name	Abbreviation
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCC
External Interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC Controller	CRC
Power management unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time Clock	RTC
External memory controller	EMMC
Controller Area Network	CAN
I2C Interface	I2C
Serial Peripheral Interface	SPI
Universal asynchronous receiver transmitter	UART
Universal synchronous and asynchronous receiver transmitter	USART
Flash interface control unit	FMC
Safe digital input/output	SDIO
Digital camera interface	DCI

10 Revision

Table 53 Document Revision History

Date	Version	Change History
December, 2025	1.0	• initial version
April, 2026	1.1	• Modified the data in the "Low Power Wake-up Time" table • Modified the data in the "Temperature Sensor Characteristics" table • Modified the system block diagram and address mapping
June, 2026	1.2	• Modified Pre-Drive to Gate driver • Modified the content of the "Gate Driver Characteristics" table
August, 2026	1.3	• Add the T7 material number

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